# Circuit Techniques for 1.5–3.6-V Battery-Operated 64-Mb DRAM

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*Abstract*—**Circuit techniques for battery-operated DRAM's which cover supply voltages from 1.5 to 3.6 V (universal $V_{CC}$), as well as their applications to an experimental 64-Mb DRAM, are presented. The proposed universal-$V_{CC}$ DRAM concept features a low-voltage (1.5 V) DRAM core and an on-chip power supply unit optimized for the operation of the DRAM. A circuit technique for oxide-stress relaxation is proposed to improve high-voltage sustaining characteristics while only scaled MOSFET's are used in the entire chip. This technique increases sustaining voltage by about 1.5 V when compared with conventional circuits and allows scaled MOSFET's to be used for the circuits, which can be operated from an external $V_{CC}$ of up to 4 V. A two-way power supply scheme is also proposed to suppress the internal voltage fluctuation within 10% when the DRAM is operated from external power supply voltages ranging from 1.5 to 3.6 V. An experimental 1.5–3.6-V 64-Mb DRAM is designed based on these techniques and fabricated by using 0.3-$\mu$m electron-beam lithography. An almost constant access time of 70 ns is obtained over a supply voltage range from 1.5 to 3.6 V. This indicates that battery operation is a promising target for future DRAM's.**

## I. Introduction

DYNAMIC random access memories (DRAM's) have been widely used in the electronics field because of their low bit cost among semiconductor memories due to their simple memory cell structure. They have been playing an important role in enhancing the performance and reducing the cost of electronic systems. The density of DRAM's has quadrupled every three years since their advent and has reached 64 Mb [1]. As the density reaches megabytes per chip, demands for DRAM's have become manifold in terms of performance and function. Battery-operated DRAM's are increasingly important in the field of battery-based systems such as notebook type personal computers (PC's) and solid-state discs (SSD's) because of the demand for low-cost and low-power semiconductor memories in such systems. SRAM's have mainly been used for these applications because: 1) the supply voltage range of DRAM's is smaller than that for SRAM's; 2) DRAM's have relatively poor immunity for $V_{CC}$ fluctuation ($V_{CC}$ bump); and 3) the operating power of DRAM's for data retention as well as for the read/write operation is comparatively large. The first and second problems stem from the strong dependence of signal-to-noise ratio (SNR) on operating voltage. The third problem is mainly due to the charging and discharging of the heavily capacitive data lines required by the refresh operation. One way to solve the third problem is to reduce the operating voltage or data-line swing [1], [2]. However, the other two issues still remain. Solving these problems would make DRAM's widely used in battery-based equipment.

This paper describes circuit techniques in achieving 1.5–3.6-V 64-Mb DRAM's to solve these issues [3]. To cover a wide range of supply voltages, the universal-$V_{CC}$ DRAM concept is proposed. The idea is to employ a low-voltage (1.5 V) operating DRAM core [1] and a two-way power supply unit to regulate the internal operating voltage against external $V_{CC}$ fluctuation. This enables the DRAM to be operated on a variety of batteries having various supply voltage levels as well as on the standard 3.3-V power supply and ensures a stable operation under long-term or short-term supply voltage fluctuation due to the battery characteristics. To achieve reliable operation, a circuit technique to relax the oxide stress of the MOSFET's is proposed. It allows the use of scaled MOSFET's for input/output buffers and the power supply unit. An experimental 1.5–3.6-V 64-Mb DRAM is designed based on these techniques and fabricated by 0.3-$\mu$m electron-beam lithography.

The universal-$V_{CC}$ DRAM concept is described in Section II. The oxide-stress relaxation technique is discussed in Section III. The design and experimental results of the two-way power supply unit are described in Section IV. Finally, the design and performance of an experimental 1.5–3.6-V 64-Mb DRAM employing these techniques are presented.

## II. Universal-$V_{CC}$ DRAM Concept

A block diagram of the universal-$V_{CC}$ 64-Mb DRAM, which covers supply voltages from 1.5 to 3.6 V, is shown in Fig. 1. The major components of the DRAM are: a

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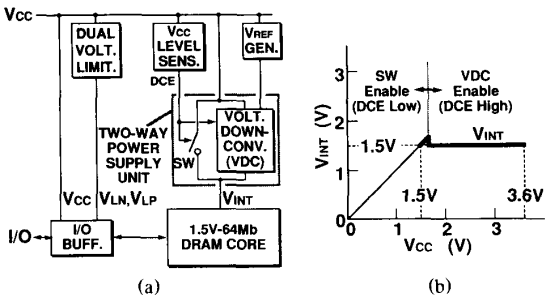



Fig. 1. Concept of universal-$V_{CC}$ DRAM: (a) block diagram of 1.5–3.6-V 64-Mb DRAM and (b) characteristics of two-way power supply unit.

TABLE 1
FEATURES OF THE EXPERIMENTAL 1.5–3.6-V 64-Mb DRAM

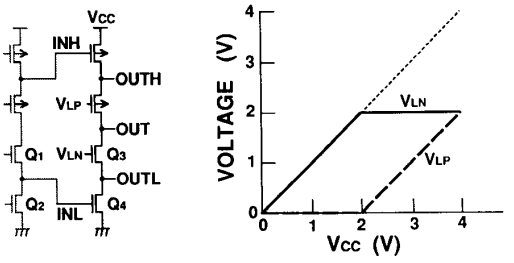
| | |
|---|---|
| Organization | 16 M Words × 4 b |
| Technology | 0.3-$\mu$m p-sub Triple-Well CMOS<br>44-fF Data-Line Shielded STC Cell<br>$T_{OX}$ = 6.5 nm<br>$L_N / L_P$ = 0.5/0.6 $\mu$m (drawn)<br>0.35/0.45 $\mu$m (effective)<br>$V_{TN} / V_{TP}$ = 0.4/−0.4 V |
| Cell size | 0.8 $\mu$m × 1.6 $\mu$m = 1.28 $\mu$m$^2$ |
| Chip size | 9.74 mm × 20.28 mm = 197.5 mm$^2$ |
| Power supply | 1.5–3.6 V (internal 1.5 V) |
| Access time | simulated $t_{RAC}$ = 50 ns<br>(1.5–3.6 V, 25°C)<br>measured $t_{RAC}$ = 70 ns<br>(1.5 and 3.3 V, 25°C) |
| Supply current | Active 29 mA at 1.5 V<br>35 mA at 3.3 V<br>($t_{RC}$ = 180 ns, 25°C)<br>Standby < 1 mA (1.5 V, 25°C) |

1.5-V 64-Mb DRAM core [1]; a dual voltage limiter for oxide-stress relaxation; a two-way power supply unit for the 1.5-V DRAM core; and high-voltage sustaining input/output buffers. One of the keys in achieving the universal-$V_{CC}$ DRAM is the low-voltage operating DRAM core. The 1.5-V 64-Mb DRAM core design is summarized in Table I. A novel crown-shaped stacked capacitor (CROWN) cell was developed to ensure enough storage charge even at 1.5 V [4]. The cell features a cylindrical storage electrode formed on the data line and a CVD-$Ta_2O_5$ dielectric film with an equivalent thickness of 3 nm [5]. A storage capacitance of more than 40 fF can be obtained even in a cell area of 1.28 $\mu$m$^2$. An important feature of the CROWN cell is that the data line is shielded by either the plate or storage layer. Inter-data-line capacitance is thereby minimized, and data-line interference noise is reduced without transposing the pair of data lines [6], [7]. Scaled MOSFET's ($t_{OX}$ = 6.5 nm, $L_{eff(min)}$ = 0.35 $\mu$m) are used to achieve high-speed performance at 1.5 V. Thus, the 1.5-V DRAM core offers enough SNR and high-speed operation using these process and device technologies. A dual voltage limiter provides two kinds of limited voltage, $V_{LN}$ and $V_{LP}$, for n-channel and p-channel MOSFET's, respectively. It enables the voltage applied to all MOSFET's to be suppressed below 2.5 V even when operating with an external supply voltage of 4 V. Scaled MOSFET's with $t_{OX}$ = 6.5 nm can be used for input/output buffers and the power supply unit. Internal supply voltage $V_{INT}$ is supplied through a two-way power supply unit which consists of a voltage down converter (VDC) and switch (SW). The reference voltage $V_{REF}$ is the reference input for the VDC. Either the VDC or SW is enabled by the control signal DCE (down converter enable), which is generated by the $V_{CC}$ level sensor. Fig. 1(b) shows the dependence of internal supply voltage $V_{INT}$ on external supply voltage $V_{CC}$. The voltage down converter works if the operating voltage is high and DCE is high, while the switch is enabled when $V_{CC}$ is decreased to around 1.5 V and DCE is low. It is best to set this switching voltage as low as possible to minimize the $V_{INT}$ fluctuation. The switching of these two means occurs when $V_{CC}$ = 1.65 V in this example. By using this two-way power supply scheme, $V_{INT}$ can be controlled within 1.5–1.65 V when supplied from external voltage ranging from 1.5 to 3.6 V. When combining these components, the SNR and operating speed of the DRAM are hardly affected by the external voltage fluctuation. Therefore, this scheme offers a stable and high-speed operation over an operating voltage range of 1.5 to 3.6 V.

## III. Oxide-Stress Relaxation Technique

One of the issues in designing a universal-$V_{CC}$ DRAM is the insufficient stress voltage sustaining characteristics of scaled MOSFET's tailored to low-voltage operation. It is difficult to achieve both high speed and reliable operation if the maximum operating voltage is two times larger than the minimum value. A dual $t_{OX}$ structure was proposed to solve this problem [8], [9]. However, it complicates both the fabrication process and device design.

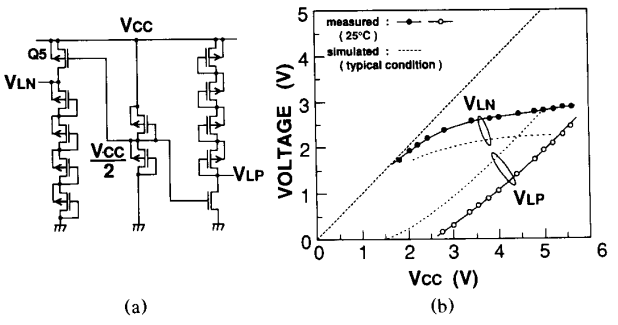
The oxide-stress relaxation technique concept using a dual-voltage-limiting scheme is presented in Fig. 2. It differs from the previously proposed hot-carrier suppression technique [10]. Its feature is to relax the stress induced by the large electric field across thin gate oxide as well as that induced by hot carrier. Fig. 2(a) shows the fundamental inverter circuit with a dual-voltage-limiting scheme. It has a symmetrical configuration like a conventional CMOS inverter. When considering the n-channel side, the main differences from a conventional one are the insertion of limiting MOSFET's $Q1$ and $Q3$ to the conventional CMOS inverter, and the output OUTL is obtained from the midpoint of the serially connected MOSFET's $Q1$ and $Q2$, or $Q3$ and $Q4$, to drive the next stage inverter. Limiting voltage for n-channel MOSFET's, $V_{LN}$, is applied to the gates of limiting n-channel MOSFET's $Q1$ and $Q3$. The p-channel side has the same configuration, and limiting voltage $V_{LP}$ is applied to the gates of limiting p-channel MOSFET's. Note that the




| | | INL=0V | INL=1.5V |
|---|---|---|---|
| OUT | | 4V | 0V |
| OUTL | | 1.5V | 0V |
| Q3 | Vgs | 0.5V | 2.0V |
| | Vds | 2.5V | 0V |
| | Vgd | 2.0V | 2.0V |
| Q4 | Vgs | 0V | 1.5V |
| | Vds | 1.5V | 0V |
| | Vgd | 1.5V | 1.5V |

(a) (b) (c)

Fig. 2. Dual-voltage-limiting scheme for oxide-stress relaxation: (a) fundamental inverter with dual-voltage-limiting scheme, (b) characteristics of dual voltage limiter, and (c) node voltages for two logic states for $V_{CC} = 4$ V, $V_{LN} = 2$ V, and $V_{TN} = 0.5$ V.




(a) (b)

Fig. 3. Dual-limiting-voltage ($V_{LN}, V_{LP}$) generator: (a) circuit schematic and (b) measured and simulated characteristics.

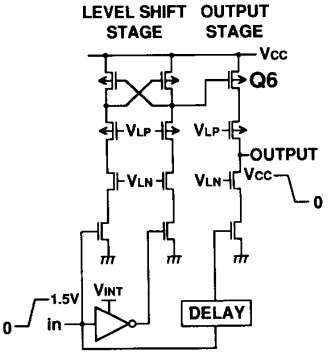



Fig. 4. Oxide-stress relaxed output buffer with dual-voltage-limiting scheme.

full-swing output OUT is obtained at the midpoint between n-channel and p-channel MOSFET's. Ideal dc characteristics of limiting voltages $V_{LN}$ and $V_{LP}$ are shown in Fig. 2(b). $V_{LN} = V_{CC}$ and $V_{LP} = 0$ V when $V_{CC} < 2$ V, while $V_{LN} = 2$ V and $V_{LP} = V_{CC} - 2$ V when $V_{CC} > 2$ V. The drain voltage of $Q4$ is limited below $V_{LN} - V_{TN}$ by $Q3$ and the high level of the output OUTL is also limited below $V_{LN} - V_{TN}$. The gate voltage of $Q4$ is also limited below $V_{LN} - V_{TN}$ by $Q1$. To show the effect of this scheme, node voltages for n-channel MOSFET's $Q3$ and $Q4$ are summarized corresponding to the two logic states, INL = "low" (0 V) and INL = "high" (1.5 V). It is assumed here that $V_{CC} = 4$ V, $V_{LN} = 2$ V, and the gate threshold voltage $V_{TN} = 0.5$ V. The maximum applied voltage between any two nodes of the n-channel MOSFET's is suppressed below 2.5 V when input is "low" and is suppressed below 2.0 V when input is "high." The maximum voltage applied between drain and source of $Q3$ is $V_{CC} - V_{LN} + V_{TN}$ when input is "low," while that applied between gate and source/drain is $V_{LN}$ when input is "high." This means that the optimum limiting voltage is $V_{LN} = (V_{CC} + V_{TN})/2$. This is the same for p-channel MOSFET's. Thus, the voltage applied to the MOSFET is almost halved by using this scheme and the oxide stress for all MOSFET's is relaxed.

The limiting voltages, $V_{LN}$ and $V_{LP}$, generating circuit is shown in Fig. 3(a). The threshold voltage of a p-channel MOSFET, $V_{TP}$, is used as the reference. The gate voltage of the $Q5$ is biased at $V_{CC}/2$ so as to relax oxide stress. Fig. 3(b) shows the measured characteristics of the limiting voltages together with the simulated ones. The difference in the characteristics is due to the threshold voltage deviation from the designed value.

The oxide-stress relaxed output buffer with dual voltage limiting scheme is shown in Fig. 4. The buffer consists of the output stage and the level-shift stage, which generates the drive signal for $Q6$. The full-swing output is obtained at the buffer output. The delay circuit is used for adjusting the delays of the drive signals for n-channel and p-channel MOSFET's of the output stage to avoid an unfavorable dc-current flow, which occurs if both n-channel and p-channel MOSFET's turn on at the same time. The level-shift stage consists of cross-coupled p-channel MOSFET's and an n-channel MOSFET pair, which is driven by the complementary signals. Fig. 5 shows a simulated transient response of the gate/drain voltages for p-channel MOSFET's in the output stage when the output is driven from "high" to "low." The simulation was performed for $V_{CC} = 3.3$ V and $V_{INT} = 1.5$ V. The simulation results show that the gate/drain voltage is suppressed below 2 V when operating from an external voltage of 3.3 V. In order to estimate the device lifetime [11], substrate currents $I_{BB}$ induced by hot-carrier generation were measured for both proposed and conventional output buffers. This is shown in Fig. 6. The ratios of the

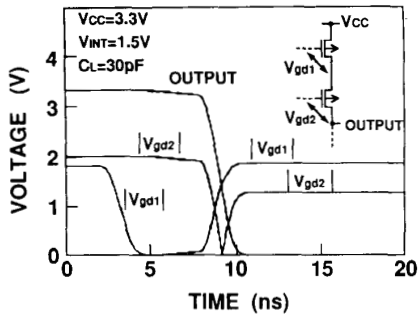



Fig. 5. Simulated transient response of gate/drain voltage for p-channel MOSFET's in output stage during switching operation of oxide-stress relaxed output buffer.

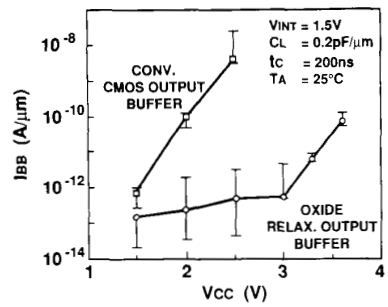



Fig. 6. Measured substrate current for conventional CMOS and oxide-stress relaxed output buffers.

load capacitance to gate width were 0.2 pF/$\mu$m for both output buffers, and the cycle time is 200 ns. The $I_{BB}$ increase was observed from 1.5 V for the conventional output buffer while it was hardly observed up to 3 V. The increase rate of the $I_{BB}$ is around two decades/0.5 V for both cases. These results indicate that the oxide-stress relaxing scheme offers a reliable operation from an external power supply voltage of up to 4 V, even by using scaled MOSFET's with a sustaining voltage as low as 2.5 V.

Another advantage of the dual-voltage-limiting scheme is to minimize dependency of speed on operating voltage. Fig. 7 shows the simulated output delay time for an oxide-stress relaxed output buffer and a conventional CMOS output buffer, for different supply voltages. An almost constant delay time was obtained for the proposed output buffer, while two times variation was obtained for the conventional CMOS output buffer. This is because the gate/source voltage of the MOSFET's in the output stage is kept almost constant in the proposed scheme. This is also advantageous in suppressing peak current for higher supply voltages. $V_{SS}$ peak currents for two kinds of output buffers were simulated as shown in Fig. 8. The device dimensions were chosen so as to get the same amount of peak current at 3.3 V. The peak current for the proposed buffer stays almost at the same level from 1.5 to 1.6 V in contrast with the strong dependence of the peak current on operating voltage for the conventional

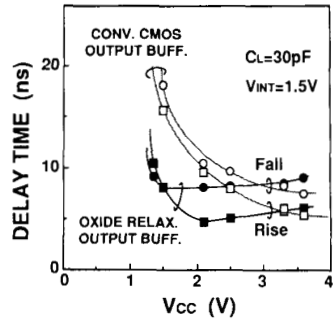



Fig. 7. Simulated output delay time for two types of output buffers for different supply voltages.

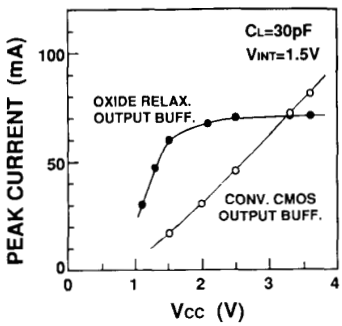



Fig. 8. Simulated $V_{SS}$ peak current for two types of output buffers for different supply voltages.

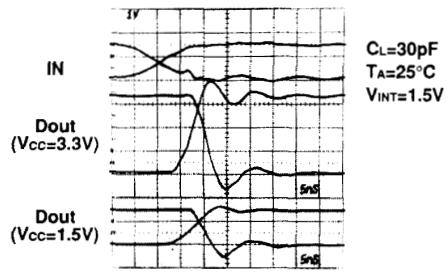



Fig. 9. Operating waveforms for oxide-stress relaxed output buffer.

buffer. This helps to suppress the noise associated with a large peak current, especially in higher $V_{CC}$ conditions. The operating waveforms of the proposed output buffer for $V_{CC} = 1.5$ and 3.3 V are shown in Fig. 9. Almost the same delay time was observed for the two different voltages, as was expected from simulation results.

## IV. Two-Way Power Supply Scheme

Fig. 10 shows a circuit schematic of the two-way power supply unit. Internal supply voltage $V_{INT}$ is fed through either the voltage down converter (VDC) or the switch (SW). The oxide-stress relaxation technique is also applied to this supply unit so miniaturized MOSFET's can be used. The VDC consists of the current-mirror differen-

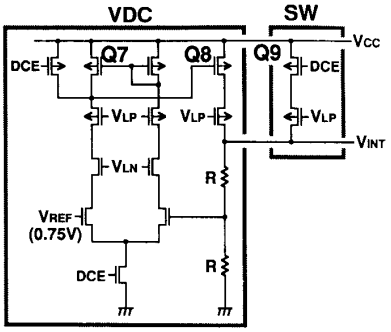



Fig. 10. Circuit schematic of two-way power supply unit.

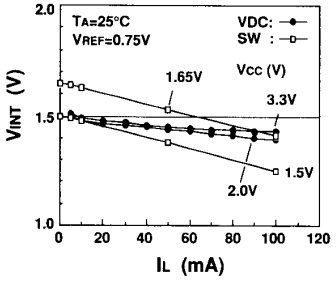



Fig. 11. Measured $V_{INT}$ versus load current characteristics for two-way power supply unit for different supply voltages.

tial amplifier and the output stage with p-channel MOSFET's. This configuration shows good voltage regularity [12]. The reference input for the VDC ($V_{REF}$) is designed to be 0.75 V (half of the $V_{INT}$) so that the common-mode input level is low enough to provide stable operation even when $V_{CC}$ decreases to around 1.5 V. This low input level prevents operation in the linear region for the p-channel MOSFET ($Q7$) of the differential stage and attains enough voltage gain when $V_{CC}$ is decreased to 1.5 V. One reason why the SW is used in the low operating voltage region is that the driving capability of $Q8$ is comparatively low when $V_{CC}$ is decreased to about $V_{INT}$ and $Q8$ operates in the linear region. The switch with p-channel MOSFET $Q9$ is then used for low supply voltage. The gate width of $Q9$ is three times larger than $Q8$ to minimize the on-resistance when $V_{INT}$ is supplied from $V_{CC}$ directly. The other reason is to save the operating power of the VDC when supply voltage is low and external $V_{CC}$ can be directly applied to the DRAM core. DCE is "high" and the VDC is enabled when $V_{CC} > 1.65$ V, while DCE is "low" and the SW is enabled when $V_{CC} < 1.65$ V. The measured $V_{INT}$ versus load current characteristics for the two-way power supply unit for different supply voltages are shown in Fig. 11. The VDC is enabled when $V_{CC} = 3.3$ and 2.0 V while the SW is enabled when $V_{CC} = 1.65$ and 1.5 V. The average operating current for the peripheral circuit of the designed 64-Mb DRAM was 16 mA with 180-ns *RAS* cycle time for a typical condition. The simulation results show that $V_{INT}$ at the output of the VDC was deviated

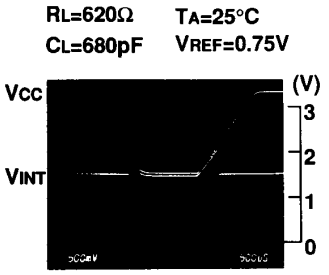
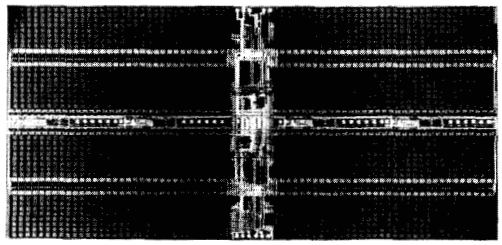



Fig. 12. Transient response of $V_{INT}$ for 1.5–3.6-V $V_{CC}$ bump.

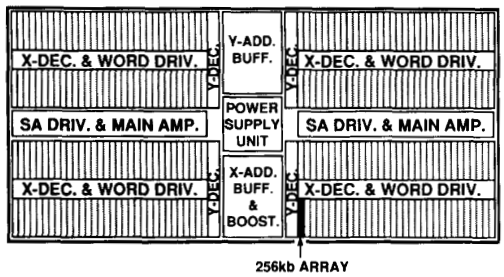
from the quiescent value by +0.04 and −0.02 V due to the peak current induced by the peripheral circuit operation when the DRAM is operated from a 3.3-V external power supply. A decrease in $V_{INT}$, induced by the load current, is also reduced to as low as −10% when the SW is enabled. Thus, the proposed power supply scheme has enough margin to feed the operating current for the 1.5-V 64-Mb DRAM core. Fluctuation of $V_{INT}$ can be suppressed to within ±10% (±0.15 V) of the quiescent value (1.5 V) over an operating voltage range of 1.5 to 3.6 V when the VDC and SW are switched at 1.65 V. Fig. 12 shows the transient response of $V_{INT}$ for a 1.5–3.3-V $V_{CC}$ bump measured using a test circuit. A dummy load with resistance and capacitance is connected at the output. The reference input voltage for the VDC was 0.75 V. Switching of the VDC and the SW is designed to occur at $V_{CC} = 1.8$ V for negative and 2 V for positive transition of $V_{CC}$. The reason for making the switching voltage different is to avoid chattering between the VDC and the SW. These values can be decreased to around 1.65 V to decrease $V_{INT}$ fluctuation. The experimental results show smooth switching characteristics between the VDC and the SW for a 1.5–3.3-V $V_{CC}$ bump.

## V. 1.5–3.6-V 64-Mb DRAM Design

An experimental 1.5–3.6-V 64-Mb DRAM was designed and fabricated utilizing the above circuit techniques. Fig. 13 shows a microphotograph and architecture of the designed chip. The chip measures 9.74 mm × 20.28 mm. The power supply unit as well as other peripheral circuits are placed in the center of the chip. This helps to shorten the internal power supply lines as well as signal lines. The simulated dependency of *RAS* access time $t_{RAC}$ on external supply voltage is shown in Fig. 14. A typical *RAS* access time of 50 ns can be obtained for an external power supply range from 1.5 to 3.6 V. Access time difference for $V_{CC} = 1.5$ and 3.3 V was reduced to as low as 1.5 ns due to proposed universal-$V_{CC}$ circuit techniques. The slight decrease in the access time for lower operating voltage is due to the reduced delay time of the output buffer as shown in Fig. 7. Typical operating current is 29 mA for 1.5-V external power supply and 35 mA for 3.3 V, both with a cycle time of 180 ns. The increase in operating current is due to that consumed by the VDC.



(a)




(b)

Fig. 13. Microphotograph and architecture of the experimental 64-Mb DRAM: (a) microphotograph and (b) chip architecture.

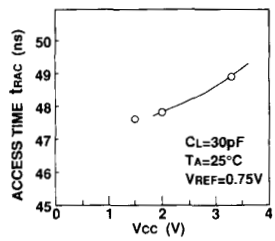



Fig. 14. Simulated *RAS* access time shown as a function of supply voltage.

Waveforms of the experimental 1.5–3.6-V 64-Mb DRAM operated from 1.5- and 3.3-V external power supply are presented in Fig. 15. A typical *RAS* access time of 70 ns was obtained for both 1.5 and 3.3 V. There are two reasons for the difference between the measured access time and the simulated one. One is a deviation in the characteristics of the MOSFET's such as the gate-oxide thickness and gate length from the designed one. The other is the deviation in the diffusion layer resistance from the designed value. Therefore, a further reduction in the access time to 50 ns is expected by improving on these drawbacks. The almost constant access time for both 1.5 and 3.3 V should be noted here. This was achieved by the circuit techniques in realizing the universal-$V_{CC}$ DRAM.

Thus, stable and high-speed operation of the DRAM can be maintained over the wide supply voltage range of 1.5–3.6 V by using the newly developed circuit techniques (universal-$V_{CC}$ DRAM) presented here.

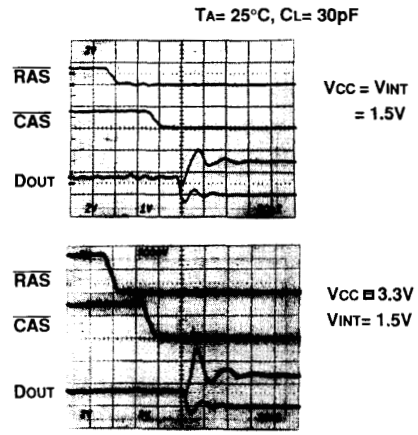



Fig. 15. Operating waveforms of the 64-Mb DRAM for 1.5- and 3.3-V external power supply.

## VI. Conclusion

Novel circuit techniques for battery-operated DRAM's which cover a wide range of operating voltage range from 1.5 to 3.6 V (universal-$V_{CC}$ DRAM) have been presented. These are the oxide-stress relaxation technique to improve high-voltage sustaining characteristics while only scaled MOSFET's are used in the entire chip, and a two-way power supply scheme to minimize the internal voltage fluctuation to achieve a stable operation over a wide supply voltage range. An increase in sustaining voltage by about 1.5 V when compared with a conventional circuit has been achieved by the oxide-stress relaxation technique. It enables scaled MOSFET's to be used for the circuits, which can be operated from an external $V_{CC}$ of up to 4 V. Internal voltage fluctuation has been suppressed to within 10% when the DRAM is operated from external power supply voltages ranging from 1.5 to 3.6 V. A 1.5–3.6-V 64-Mb DRAM has been designed using these techniques. An almost constant *RAS* access time has been obtained for 1.5–3.6-V external power supply voltages. These results show that the battery-operated DRAM is a promising target for future DRAM's.

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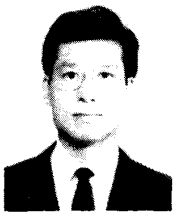

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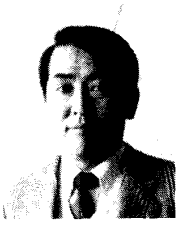

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